PACT Processor Patents

		Headline	Link	Notes
US	8 156 284	Data processing method and device	http://www.google.com/patents/US8156284	
US	8 145 881	Data processing device and method	http://www.google.com/patents/US8145881	
US	8 127 061	Bus systems and reconfiguration methods	http://www.google.com/patents/US8127061	
US	7 996 827	Method for the translation of programs for reconfigurable architectures	http://www.google.com/patents/US7996827	
US	7 928 763	Multi-core processing system	http://www.google.com/patents/US7928763	
US	7 657 877	Method for processing data	http://www.google.com/patents/US7657877	
US	7 657 861	Method and device for processing data	http://www.google.com/patents/US7657861	
US	7 602 214	Reconfigurable sequencer structure	http://www.google.com/patents/US7602214	
US	7 584 390	Method and system for alternating between programs for execution by cells of an integrated circuit	http://www.google.com/patents/US7584390	
US	7 581 076	Methods and devices for treating and/or processing data	http://www.google.com/patents/US7581076	
US	7 577 822	Parallel task operation in processor and reconfigurable coprocessor configured based on information in link list including termination information for synchronization	http://www.google.com/patents/US7577822	
US	7 434 191	Router	http://www.google.com/patents/US7434191	
US	7 394 284	Reconfigurable sequencer structure	http://www.google.com/patents/US7394284	
US	7 010 667	Internal bus system for DFPS and units with two- or multi-dimensional, programmable cell architectures, for managing large volumes of data with a high interconnection complexity	http://www.google.com/patents/US7010667	
US	7 003 660	Pipeline configuration unit protocols and communication	http://www.google.com/patents/US7003660	
US	6 990 555	Method of hierarchical caching of configuration data having dataflow processors and modules having two- or multidimansional programmable cell structure (FPGAs, DPGAs, etc.)	http://www.google.com/patents/US6990555	
US	6 697 979	Method of repairing integrated circuits	http://www.google.com/patents/US6697979	
US	6 687 788	Method of hierarchical caching of configuration data having dataflow processors and modules having two- or multidimansional programmable cell structure (FPGAs, DPGAs, etc.)	http://www.google.com/patents/US6687788	
US	6 571 381	Method for deadlock-free configuration of dataflow processors and modules having two- or multidimansional programmable cell structure (FPGAs, DPGAs, etc.)	http://www.google.com/patents/US6571381	
US	6 480 937	Method for hierarchical caching of configuration data having dataflow processors and modules having two- or multidimansional programmable cell structure (FPGAs, DPGAs, etc.)	http://www.google.com/patents/US6480937	
US	6 405 299	Internal bus system for DFPS and units with two- or multi-dimensional, programmable cell architectures, for managing large volumes of data with a high interconnection complexity	http://www.google.com/patents/US6405299	FPGA too
US	6 038 650	Method for the automatic address generation of modules within clusters comprised of a plurality of these modules	http://www.google.com/patents/US6038650	

PACT Processor Patent Applications

	Application	Notes
	12/495,465	
	12/840,477	
	12/944,068	
	13/043,102	
	11/122,500	allowed
	10/501,845	
	12/570,984	
	10/501,903	
	12/729,090	
	12/729,932	
	12/570,943	
	10/490,081	
	12/571,173	
	12/621,860	
	13/040,769	
	12/947,167	
	10/551,891	
	12/571,195	
	11/883,670	
	13/026,475	
	12/743,356	
	12/745,335	